**WHAT IS CLAIMED IS:**

1. A test circuit including at least one test channel input, each test channel input being adapted to receive respective encoded test channel data and the test circuit including configuration inputs adapted to receive configuration signals and further including a plurality of decoded outputs, the test circuit being programmable responsive to the configuration signals to execute a desired decoding algorithm, and being operable to apply the decoding algorithm to the encoded test channel data from each test channel input and to develop decoded test data, the decoded test data including N bits and the encoded test channel data including M bits, where N is greater than M, and the test circuit applying the decoded test data bits on the decoded outputs.

2. The test circuit of claim 1 wherein the test circuit comprises an FPGA.

3. The test circuit of claim 1 wherein the test circuit operates in a scan test mode and a functional test mode responsive to the configuration signals, and wherein the test circuit executes different decoding algorithms during the scan and functional test modes.

4. The test circuit of claim 3 wherein the test circuit couples each test channel input to a plurality of decoded outputs to define the decoding algorithm executed during the scan test mode.

5. The test circuit of claim 1 wherein M<N<2^(M+1).

6. A test system, comprising:

a tester operable to provide encoded test channel data on at least one test channel output;

a test circuit including at least one test channel input, each test channel input being coupled to a corresponding test channel output to receive encoded test channel data and the test circuit including configuration inputs adapted to receive configuration signals and further including a plurality of decoded outputs, the test circuit being programmable responsive to the configuration signals to execute a desired decoding algorithm, and being operable to apply the decoding algorithm to the encoded test channel data from each test channel input and to develop decoded

test data, the decoded test data including N bits and the encoded test channel data including M bits, where N is greater than M, and the test circuit applying the decoded test data bits on the decoded outputs; and

a device under test including circuitry and including a plurality of pins coupled to the circuitry, and at least some of the pins being coupled to the decoded outputs of the test circuit to receive decoded test data bits.

7. The test system of claim 6 wherein the test circuit comprises an FPGA.

8. The test system of claim 6 wherein the tester applies the configuration signals to the test circuit.

9. The test system of claim 6 wherein the test circuit operates in a scan test mode and a functional test mode responsive to the configuration signals, and wherein the test circuit executes different decoding algorithms during the scan and functional test modes.

10. The test system of claim 9 wherein the test circuit couples each test channel input to a plurality of decoded outputs to define the decoding algorithm executed during the scan test mode.

11. The test system of claim 6 wherein the test circuit is physically formed within the device under test, and wherein the test channel inputs and configuration inputs of the test circuit are coupled to pins of the device under test.

12. The test system of claim 11 wherein the test circuit operates in a scan test mode and a functional test mode responsive to configuration signals applied to corresponding pins of the device under test, and wherein the test circuit executes different decoding algorithms during the scan and functional test modes.

13. The test system of claim 6 wherein the tester further includes test data inputs and address and control outputs coupled to pins on the device under test, and wherein the develops signals on the address and control outputs to transfer decoded test data into the device under test via the test circuit, and wherein the device under test provides results test data on the test data inputs and the tester operates to analyze the test data to detect defects in the device under test.

14. The test system 6 wherein the test circuit and device under test collectively form a test bench, and wherein the tester provides an initialization signal to the test circuit on a test channel output and wherein, responsive to the initialization signal, the test circuit generates the configuration signals to execute the desired decoding algorithm and applies the decoded test data on the test channel inputs, the test circuit being further operable to apply address and control signals along with the decode test data to the device under test, wherein the device under test executes a test responsive to the address and control signals and decoded test data and applies a signature signal to the test circuit indicating the results of the test, and wherein the test circuit, responsive to the signature, processes the signature and applies a status signal to the tester indicating the results of the test.

15. The test system of claim 14 wherein the test circuit comprises an FPGA.

16. A method of testing a device under test having a plurality of pins M with a tester having a plurality of test channels N, where N is less than M, the method comprising:

coupling a plurality of pins on the device under test to the test channels on the tester;

transferring test data into the device under test over the test channels coupled to the pins on the device under test;

testing the device under test using the transferred test data; and

providing from the device under test an indication of the results of the test.

17. The method of claim 16 wherein testing the device under test using the transferred test data comprises executing a scan test in the device under test.

18. The method of claim 16 wherein providing from the device under test an indication of the results of the test comprises compacting internal test data within the device under test to generate a signature and providing the signature from the device under test.

19. A method of testing a device under test having a plurality of external pins M with a tester having a plurality of test channels N, where N is less than M, the method comprising:

applying test data on each of the test channels, the test data on each channel including X bits;

generating from the test data applied on each test channel expanded test data having Y bits, where Y is greater than X;

applying the respective bits of expanded test data on Y external pins of the device under test;

testing the device under test using the expanded test data applied on the pins; and

providing from the device under test an indication of the results of the test.

20. The method of claim 19 wherein generating from the test data applied on each test channel expanded test data and applying the respective bits of the expanded test data comprise:

during a scan test mode of operation,

generating expanded test data having a first group of Y bits;

applying the respective bits of expanded test data in the first group on a first group of Y external pins of the device under test;

during a functional test mode of operation,

generating expanded test data having a second group of Y bits;

applying the respective bits of expanded test data in the second group on a second group of Y external pins of the device under test.

21. The method of claim 20 wherein the first group of Y bits is different than the second group of Y bits and wherein the second group of Y external pins is the same as the first group of Y external pins.

22. The method of claim 19 wherein testing the device under test using the expanded test data applied on the pins comprises executing a scan test in the device under test.

23. The method of claim 19 wherein providing from the device under test an indication of the results of the test comprises compacting internal test data within the device under test to generate a signature and providing the signature from the device under test.